Abstract

In a system in which a CPU contained LSI and an external CPU share a bus, when the external CPU accesses a device to be controlled which is connected to a bus, the access to a device mounted on the common bus is not prevented in the CPU contained LSI.

A CPU contained LSI includes a CPUa, common address/data buses 111 and 112 connected to the CPUa, CPUb address/data buses 211 and 212 connected to a CPUb, and a bus adjusting circuit 105 disposed between the common address/data buses and the CPUb address/data buses to exclusively control accesses from the CPUa and the CPUb to a device connected to the common address/data buses and connect the CPUb adress/data buses to the common address/data buses only when the CPUb is permitted to access the device connected to the common address/data buses.